lattice dimension SiGe layer **41** and a second strained semiconducting layer **44** is epitaxially grown atop the second lattice dimension SiGe layer **42**. The first and second strained semiconducting layers **43**, **44** comprise epitaxially formed Si.

Similar to the previous embodiment, the first and second strained semiconducting layers **43**, **44** comprise an internal tensile stress that results from the lattice mismatch between the smaller lattice dimension of epitaxially grown Si of the first and second semiconducting layers **43**, **44** being formed atop the larger lattice dimension of the first and second lattice dimension SiGe layer **41**, **42**.

Preferably, the lattice mismatch between unstrained semiconducting layer **43** and the first lattice dimension SiGe layer **41** increases pFET device improvements and the lattice mismatch between the unstrained semiconducting layer **44** and the second lattice dimension SiGe layer **41** does not degrade nFET performance. The strain produced in the first or second strained semiconducting layer **43**, **44** is maintained so long as the first or second strained semiconducting layer **43**, **44** is not grown to a thickness greater than its critical thickness.

In a preferred embodiment, the crystallographic orientation of the first lattice dimension SiGe layer **41** is (110). Although a (110) crystal plane is preferred, the first lattice dimension SiGe layer **41** may alternatively have a (111) or a (100) crystal plane. Since the first lattice dimension SiGe layer **41** is preferably in a (110) crystal plane, the crystallographic orientation of the second lattice dimension SiGe layer **42** is preferably in a (100) crystal plane. Although a (100) crystal plane is preferred, the second lattice dimension SiGe layer **42** may alternatively have a (111) or a (110) crystal plane.

Still referring to FIG. **19**, the resulting structure comprises a substantially planar SOI substrate including a first device region **24** having a first strained semiconducting layer **43** with a first crystallographic orientation and a second device region **22** having a second strained semiconducting layer **44** with a second crystallographic orientation, the first crystallographic orientation being different from the second crystallographic orientation. Preferably, the first strained semiconducting layer **43** has a crystallographic orientation and internal tensile stress for pFET device optimization. The second strained semiconducting layer **44** of the second device region **22**, preferably has a crystallographic orientation and internal stress for nFET device optimization. The substantially planar substrate **51** may then be further processed using conventional MOSFET processing steps to form at least one pFET device **52** in first device region **24** and at least one nFET device **53** in the second device region **22**.

While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made with departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

What is claimed is:

1. A method of forming a semiconductor substrate comprising:

providing an initial structure having a first device region and a second device region positioned on and separated by an insulating material, said first device region comprising a first orientation material and said second device region comprising an insulating layer atop a second orientation material;

wherein said first orientation material and said second orientation material have a different crystallographic orientation;

forming a first concentration of lattice modifying material atop the first orientation material;

removing said insulating layer;

forming a second concentration of said lattice modifying material atop said second orientation material;

intermixing said first concentration of lattice modifying material with said first orientation material to produce a first lattice dimension surface and said second concentration of lattice modifying material with said second orientation material to produce a second lattice dimension surface; and

forming a first strained semiconducting layer atop said first lattice dimension surface and a second strained semiconducting layer atop said second lattice dimension surface, wherein said first strained semiconducting layer and said second strained semiconducting layer have said different crystallographic orientation.

2. The method of claim **1** wherein said first strained semiconducting layer has a (110) crystallographic orientation and said second strained semiconducting layer has a (100) crystallographic orientation.

3. The method of claim **2** wherein said first concentration of lattice modifying material comprises SiGe having a Ge concentration ranging from about 0% to about 100%, by atomic number % and said second concentration of lattice modifying material comprises SiGe having a Ge concentration ranging from about 0% to about 100%, by atomic number %.

4. The method of claim **3** wherein said first concentration of lattice modifying material is different than said second concentration of lattice modifying material and said first strained semiconducting layer has a different internal stress than said second strained semiconducting layer.

5. The method of claim **3** wherein said first concentration of lattice modifying material is the same as said second concentration of lattice modifying material and said first strained semiconducting layer has a same internal stress as said second strained semiconducting layer.

6. The method of claim **1** wherein providing said initial structure comprises the steps of:

providing a bonded substrate comprising an upper layer of said second orientation material and a lower layer of said first orientation material separated by said insulating layer;

protecting a portion of said bonded substrate while leaving another portion of said bonded substrate unprotected;

etching said unprotected portion of said bonded substrate to expose a surface of said lower layer of said first orientation material;

wherein a remaining portion of said upper layer of said second orientation material and said insulating layer define said second device region;

forming insulating material around said second device region;

regrowing said first orientation material on an exposed surface of said lower layer of said first orientation material to produce said first device region;

planarizing a surface of said first orientation material of said first device region substantially planar with said remaining portion of said upper layer of said second orientation material;